Charge induced pattern distortion in low energy electron beam lithography

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Charge induced pattern distortions in low voltage electron beam lithography in the energy range of 1 to 5 kV were investigated. Pattern distortion on conducting substrates such as silicon was found to be small, while significant pattern placement errors and pattern distortions were observed in the case of electrically insulating substrates caused by charge trapping and deflection of the incident electron beam. The nature and magnitude of pattern distortions were found to be influenced by the incident electron energy, pattern size, electrical conductivity, and secondary electron emission coefficient of the substrate. Theoretical modeling predicts the electron beam deflection to be directly proportional to the trapped surface charge density and inversely proportional to the accelerating voltage. © *2000 American Vacuum Society.* [S0734-211X(00)14506-8]

I. INTRODUCTION

Low voltage electron beam (LVEB) lithography is one of the techniques considered for the fabrication of nanoscale devices.[1–5] Microcolumn arrays of electron beam sources for high throughput e-beam lithography are being developed.[6] These microcolumns, due to their small size, cannot be operated above a few thousand volts. Despite similar operating principles, LVEB lithography is different from conventional high energy lithographic methods in terms of processing issues such as resist sensitivity, dose profile, proximity effects, and distortions due to charging. In particular, charge induced pattern distortion is rendered all the more important in LVEB lithography as electrons with low velocity and reduced penetration depth lead to increased charge trapping in the resist layer, compounded by substantial positive surface charge due to the increased secondary electron emission. Although a few of the recent studies investigated several aspects of low energy e-beam lithography,[2,7–10] the factors affecting charge induced pattern distortions have not been investigated in detail. Kudryashov *et al.*[11] and Liu *et al.*[12] reported charge induced pattern distortions in the low energy regime for resist thickness greater than 200 nm, which is far greater than the typical electron penetration depth of 50 nm at 1 kV. Moreover, thin resist layers increase the influence of the substrate electrical conductivity on the charge dissipation process. Here, we report experimentally observed charge induced pattern distortion in the LVEB lithography process for a beam energy in the range of 0.75 to 5 kV in structures employing a 40 nm thick resist layer on various substrates such as Si, SiO_2 coated Si (SiO_2/Si), glass, sapphire, and Cr on glass. These substrates have different secondary electron emission coefficients and electrical conductivities. Charge induced pattern distortions were also evaluated by numerical modeling.

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II. EXPERIMENT

Electron beam exposures were carried out using a thermally assisted field emission digital scanning electron microscope (Leo DSM982, SEM) controlled by a pattern generator. For electron beam exposure, the samples were grounded on a metal holder. Patterns were exposed at electron beam energies of 1, 2, and 5 kV using the critical line dose of 0.2, 0.4, and 1 nC/cm, respectively. An area dose of 30 μmC/cm^2 was used at all beam energies. A 40 nm thick poly(methylmethacrylate) (PMMA) resist layer was used on all substrates. The resist layer was prebaked at 170 °C for 30 min on a hotplate. The exposed patterns were developed in a 1:3 mixture of methyl isobutyl ketone and isopropyl alcohol for 60 s. Charge induced pattern placement errors were measured employing a SEM after depositing a thin gold layer on the sample or after the metal lift off of 20 nm gold films.

III. LINE DEFLECTION MEASUREMENTS

A schematic of the test pattern layout used to measure the pattern displacement is shown in Fig. 1, which consists of three single pass lines *A, B, C* and a charge pad *S*. Lines *A* and *B* are the reference lines and *C* is the test line. The reference lines were exposed first followed by the exposure of charge pad *S*. The test line *C* was exposed immediately after writing the charge pad. The displacement of the exposed line *C* with respect to its position defined in the pattern layout indicates the pattern deflection due to the charge trapped in the charge pad. The measured difference in the distance between lines *A* to *B* and lines *B* to *C* is the actual line deflection. This method eliminates the error due to small geometrical distortions of the exposure field. The line deflection measurements were carried out using the image analysis routine of the Leo SEM system. The line deflection and the standard deviation were obtained by measuring the distance between lines *A* to *B* and *B* to *C* at ten different locations using the high magnification SEM images. The exposure was done on a minimum of three sets of samples at each condition.

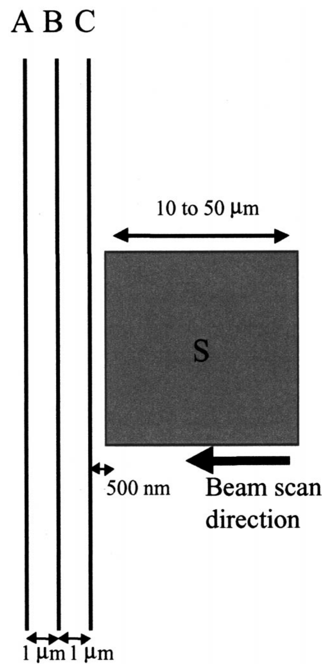

FIG. 1. Schematic of the test pattern layout, where lines *A, B*, and *C* are the single pass lines with line separation of 1 μm. *S* is the charge pad. Line *C* is the test line placed at a distance of 0.5 μm from the left-hand side edge of the charge pad *S*. While exposing charge pad, the beam was scanned from the right-hand side to the left-hand side as indicated by the arrow.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

Figures 2(a) and 2(b) show the SEM images of the single pass lines *A, B*, and *C* of a pattern having a 30 μm $\times$30 μm charge pad (not shown in Fig. 2) exposed at 2 kV on silicon and glass, respectively. The deflection of the test line *C* towards the reference line *B* (and away form the charge pad) in Fig. 2(b) suggests that the charge trapped in the charge pad is of negative polarity on the substrate. On silicon, the maximum line deflection obtained was less than 20 nm and the line deflection showed no significant dependence on the charge pad size or electron beam energy. This deflection includes an uncertainty of $\sim$10 nm due to the line edge roughness, pixel size, and the placement accuracy of the pattern generator. The resist thickness used here was smaller than the penetration depth of 1 kV (50 nm) electrons

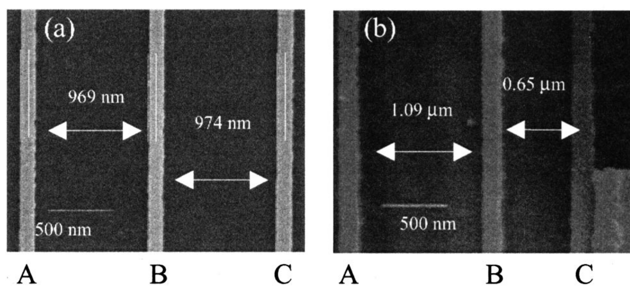

FIG. 2. High magnification SEM images of the single pass lines on (a) silicon and (b) glass for a pattern having 30$\times$30 μm charge pad (not shown) exposed at 2 kV with a line dose of 0.4 nC/cm and an area dose of 30 μC/cm^2.

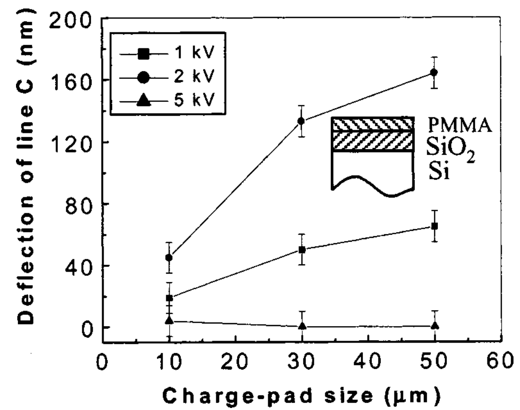

FIG. 3. Variation of line deflection as a function of charge pad edge length for patterns exposed at different beam energies using 40 nm PMMA on 480 nm thick SiO_2 coated Si.

and the deposited charge apparently dissipates through, or is well shielded by, the grounded substrate. Further, the time taken to expose the charge pad is much larger than both the time required for the charge to dissipate through the silicon substrate and the time required for the partial screening by the charges in the substrate. Therefore the net-trapped charge is small leading to negligible pattern placement error. This observation is similar to that of high energy electron beam lithography.[13]

No significant line deflection or pattern distortion was observed on patterns exposed on a silicon substrate coated with a 200 nm thick SiO_2 film. Patterns exposed on a silicon substrate having 480 nm thick SiO_2 layer showed significant line deflection 2 kV. The deflection of the test line *C* towards the reference line *B* and away from the charge pad implies that the charge trapped in the charge pad is of negative polarity on this substrate. Figure 3 shows the variation of line deflection as a function of charge pad size. At 2 kV, the line deflection significantly increased with an increase in the charge pad size. At 5 kV, the observed line deflections were small and this could be due to the longer penetration depth of 5 kV electrons.

A large line deflection and distortion in the charge pad shape was observed in patterns exposed on glass. The deflection shown in Fig. 2(b) suggest that the trapped charge is of negative polarity. Figure 4(a) shows the variation of line deflection with charge pad size as a log–log plot. The line deflection increased with an increase in the charge pad size and the beam energy. At 1 kV, measured line deflection was less than 20 nm for a pattern having 10 μm$\times$10 μm charge pad, whereas a pattern having 50 μm$\times$50 μm charge pad showed a line deflection of 500 nm. The log–log plot of the deflection as a function of the charge pad size is expected to show a linear relation for a charge pad size much smaller than the working distance.[13] On glass, the deflection seems to flatten out for large pad sizes. This observation suggests that some amount of charge is dissipating and could be due to the electron beam induced conductivity.[14]

Also, on sapphire a large line deflection and pattern distortion were observed. The charge trapped in the charge pad

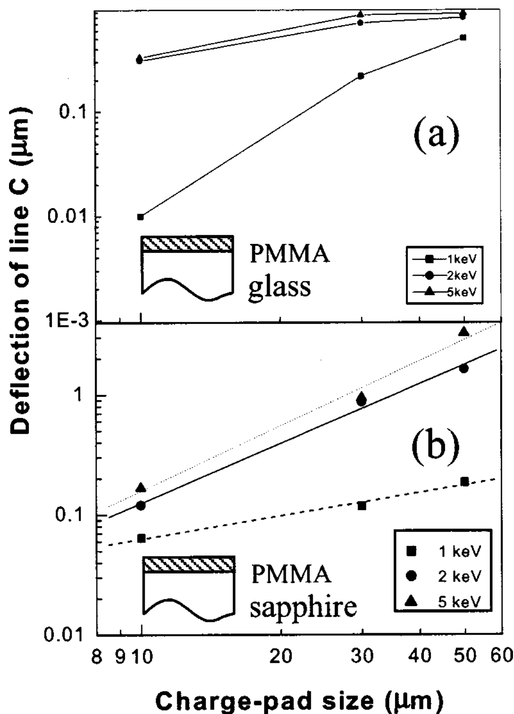

FIG. 4. Log–log plot of line deflection as a function of charge pad edge length for patterns exposed at different beam energies using 40 nm PMMA on (a) glass and (b) sapphire.

is of negative polarity as in the other cases. Figure 4(b) shows the log–log plot of line deflection as a function of charge pad size. The log–log plot shows a linear behavior suggesting that the charge leakage is small on sapphire unlike in the case of glass. At 1 kV, the line deflection was small and this could be due to the increased secondary electron emission of sapphire at 1 kV.[15]

Further, the effect of a metal interlayer on charging was also investigated. Patterns were exposed in PMMA on 80 nm thick Cr layer on glass. No charge induced pattern distortion was observed for a resist layer of a thickness of 40 nm. However, patterns exposed on 210 nm thick resist layer showed significant line deflection due to negative charging at 2 kV. In conventional e-beam lithography processing of insulating substrates, a conducting layer can be placed on top of the resist layer to reduce the charge induced pattern distortions.[16] The smaller penetration depth of low energy electrons imposes restrictions on using a conducting overlayer for charge reduction. Our study on a Cr-coated glass substrate shows that if the resist thickness is smaller than the electron penetration depth, a conducting underlayer can be used on insulating substrates to reduce the charge induced pattern distortions in LVEB processing. Our observation suggests that chrome coated masks can be patterned by low energy electron beam lithography without charge induced pattern placement errors.

The difference in the extent of charge induced pattern distortion on different substrates seems to be mainly due to the difference in their electrical conductivity and the secondary electron emission coefficient. Even though a positive surface charge density is expected at low electron beam energies, the observed negative charge density on glass and sapphire agree well with the earlier reports on negative charging.[17,18] The line deflection and the distortions in patterns exposed on sapphire are two to three times larger than that on glass. It should be noted that the electrical resistivity of sapphire is greater than 10^{15} Ω cm and that of silicate glass is $\sim 10^{12}$ Ω cm.

Kudryashov *et al.*[11] observed a large negative charge induced deflection at 3 kV and a reduced deflection for lower energies (<3 kV) for a 1 μm thick PMMA resist. They explained their results on the basis of increased secondary electron emission at lower energies where a positive surface charge density is expected for beam energies smaller than 1.5 kV. Further, Liu *et al.*[12] observed a positive surface potential at electron beam energies greater than 6 kV and a negative surface potential at electron beam energies smaller than 6 kV for a 0.4 μm thick polybutene sulfone (PBS) and SAL601 resists coated on Cr/glass substrate. Recently, Bai *et al.*[19] reported an increase in the positive surface potential with an increase in the beam energy and decrease in the resist thickness for PBS and UV5 resists on silicon substrate. According to these reports, when the resist thickness is smaller than the electron penetration depth, the trapped negative charge is negligible as the conducting substrate gives rise to image charges. On the other hand, secondary electrons escaping from the top surface lead to a net positive surface potential. These observations suggest that a resist thickness less than the penetration depth (for 1–5 kV) employed in the present study would show a small net positive surface potential. However, our data did not show measurable line deflection due to positive charging even in the case of conducting substrates.

V. MODELING

We also modeled the deflection of the electron beam, which results in pattern placement errors, for the experimental conditions previously described. It has been shown earlier that the beam deflection is due to charge accumulating in the resist as well as the interaction with dipoles.[11,13] These two sources of deflection are comparable for thick (>1 μm) resists. The resists we used in the present study are a factor of 10 to 30 thinner. Therefore, we expected the relative contribution from the dipole term to be small on conducting substrates and we considered only the deflection due to the charge accumulated in the resist. The approximations of the model were: (i) the resist is thin compared to the working distance and the charge pad size, (ii) the exposed area is uniformly charged in the *xy* plane, (iii) accelerating voltage is large compared to the charge-induced voltage on the pad, and (iv) the deflection is small compared to the distance from the center of charge distribution. All of these approximations hold with a high degree of accuracy for typical exposure parameters. The forces on incident electrons due to charges in the pad were calculated, and then velocities and displacements were calculated by numerical integration. This approach, rather than analytical approximations, allowed us to

calculate beam deflection for any pattern geometry. The lateral deflection of the electron beam near a square was found to be

$$\text{Deflection} = \frac{1}{8\pi\epsilon_0}\frac{\sigma}{V}\int_{z_0}^{0}\left[\int_0^{l_{sq}}\int_{-l_{sq}/2}^{l_{sq}/2}\int_{z_0}^{z_t}\frac{x+d_0}{((x+d_0)^2+y^2+z^2)^{3/2}} \times dx\,dy\,dz\right]dz_t,$$

where d_0 is the intended separation between line C and the charge pad, l_{sq} is the pad size, V is the accelerating voltage, σ is the surface charge density, z_0 is the working distance, and z_t is the intermediate integration variable. The terms within the integral represent the geometry dependent factor. This numerical result was tested against an analytical calculation for a limiting case of a very small pad. An interesting outcome is that the deflection is independent of the charge and the mass of the particles. Ions have higher mass than electrons and, therefore, are more difficult to deflect, but they also move slower, and thus are being acted on by the deflection force longer. The deflection is also very weakly dependent on the distance from the charge pad as long as the distance is smaller than the charge pad size.

The experimental value of deflections for Si, SiO_2/Si, and Cr/glass substrates were under 15–20 nm even for the largest ($50\ \mu m \times 50\ \mu m$) charge pad. Thus, we can estimate the upper limit of the effective charge density and predict the deflection for an even larger charge pad. Taking the deflection of 15 nm on silicon for a 2 kV exposure of $50\ \mu m \times 50\ \mu m$ charge pad, the corresponding charge density is -0.34 nC/cm^2 and the resulting surface potential is about 8 mV. Note that this charge density is much smaller than the deposited dose of 30 $\mu C/cm^2$, which means that most of the charge leaks away, shielded by the substrate, or results from secondary electrons rather than primary electrons. The leftover 0.34 nC/cm^2 corresponds to a 1.9×10^3 V/cm electric field. If all deposited charge, plus some fraction of secondary electrons, stayed in the resist, it would result in the field strength of $\sim 10^8$ V/cm, which is unrealistic (it results in $\sim$600 V drop over 40 nm of resist).

We did similar fits to the experimental data for glass and sapphire substrates. The calculated surface charge density and the corresponding negative surface potential on sapphire are 43 nC/cm^2 and 1 V, respectively, for the maximum deflection at 2 kV. The variation of line deflection as a function of pad size is a straight line that flattens out when the square size approaches the working distance, where the charge pad acts as an infinite half plane. The model also shows that changes in the working distance have a negligible effect on the deflection until the working distance is reduced to less than ten times the largest feature sizes.

VI. SUMMARY

Charge induced pattern distortions on different substrates were investigated in the electron beam energy range of 0.75 to 5 kV using a 40 nm thick PMMA resist. The experimental observation and theoretical modeling indicate that on low resistivity substrates such as silicon the net-trapped charge is negligible and the patterns do not suffer from significant charge induced pattern distortions. Further, charge induced pattern distortions were small on 200 nm thick SiO_2 films on silicon. The desired pattern accuracy required to match industrial standards is $<$10 nm; the 20 nm limit observed on these substrates is an upper bound on the pattern distortions. The authors believe that more precise distortion measurements are likely to result in distortions compatible with industry standards. Patterns on bulk insulating substrates showed significant pattern placement errors and pattern distortions. The extent of distortion is related to the amount of charge trapped in the charge pad. This depends on the conductivity, defect density, and secondary electron emission coefficient of the substrates, electron beam energy, and the amount of deposited charge. The study also shows that the charge induced pattern distortions in insulating substrates can be reduced by using a metal interlayer as demonstrated in the case of Cr/glass substrates.

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